IN THE SPECIFICATION:

Please amend paragraph number **[0002]** as follows:

[0002] State of the Art: As is well known, state of the art semiconductor memory and processing devices include multiple layers of electronic features which must be fabricated using multiple process steps. Individual features of state of the art semiconductor devices are generally defined by ~~photolithograpic~~ photolithographic processes wherein a resist is applied over the surface of a semiconductor substrate, or a material layer overlying a semiconductor substrate, and individual device features are patterned into the resist using a mask or reticle. After patterning the resist, the device features are permanently defined in the material layer being processed or the underlying semiconductor substrate by wet or dry etch steps. Advanced processes used to fabricate state of the art semiconductor devices may require as many as fifteen or more separate patterning and etching steps at varying layers during the fabrication process. However, in order to consistently fabricate functional and reliable semiconductor devices, it is necessary that each pattern be accurately aligned over the semiconductor substrate or material layer being processed and the feature dimensions must be precisely defined at each patterning and etch step. This is particularly true for state of the art semiconductor devices which require tolerances in the tens of nanometers range.

Please amend paragraph number **[0006]** as follows:

[0006] Depicted in drawing FIG. 2 is a ~~cross section~~ cross-section taken at line A-A of drawing FIG. 1, illustrating an overlying material layer 16 deposited over the surface 18 of the semiconductor substrate 14 after formation of the trench 11 defining the overlay target. As can be seen in drawing FIG. ~~2. The~~ 2, the overlying material layer 16 tends to conform to the topography created by the trench 11. Such conformation results in the formation of depressions 20 at the upper surface 22 of the overlying material layer 16. Even after a polishing step, portions 24 (shown in drawing FIG. 3) of the depressions 20 may still remain and serve as collection points for process residue 26 (also shown in FIG. 3), such as hemispherical grain ("HSG") Poly. As is shown in drawing FIG. 4, because the residue 26 overlies the trench 11

defining overlay target 10, the residue 26 works to obscure the outlines (depicted by dashed lines 28a and 28b) of the pattern formed by the trench 11, making the outlines 28a and 28b of the overlay target 10 to appear ragged or inconsistent. Though ~~drawing~~ drawings FIG. 2 through ~~drawing~~ FIG. 4 depict features associated with a trench-type overlay target, intermittent collection of obscuring residue is also an issue of pad-type overlay targets and overlay targets including one or more trenches or pads.

Please amend paragraph number **[0009]** as follows:

[0009] The method of forming a residue-free overlay target of the present invention may be accomplished and modified using process technology known in the semiconductor fabrication art. The method of the present invention includes providing a semiconductor substrate having top and bottom surfaces, depositing a resist layer, exposing the resist layer using a mask or reticle creating a resist pattern corresponding to at least one overlay target according to the present invention, developing ~~said~~ the resist pattern, and executing a wet or dry etch to create at least one overlay target including a trench or pad area including a series of raised lines. As will be understood by those of skill in the art, the method of the present invention may be used to create overlay targets having a variety of patterns suitable for different semiconductor device fabrication processes, as well as different manual or automated registration tools. Moreover, the method of the present invention is easily modified for the fabrication of overlay targets in a variety of substrates.

Please amend paragraph number **[0012]** as follows:

[0012] FIG. 1 provides a top view of a portion of a prior art semiconductor wafer including an overlay target and a portion of the chip pattern formed on the semiconductor wafer;

Please amend paragraph number **[0013]** as follows:

[0013] FIG. 2 depicts a ~~cross-section~~ cross-section of a portion of the prior art structure illustrated in FIG. 1, the ~~cross-section~~ cross-section being taken at line A-A of FIG. 1 and after an additional material layer is formed over the overlay target;

Please amend paragraph number **[0014]** as follows:

[0014] FIG. 3 depicts the same prior art structure as shown in FIG. 2 after the additional material layer has undergone a polishing process;

Please amend paragraph number **[0015]** as follows:

[0015] FIG. 4 provides a top view of the same portion of a prior art semiconductor wafer as is depicted in FIG. 1 after an additional material layer has been deposited over the overlay target and the additional material layer has been subjected to a polishing step;

Please amend paragraph number **[0017]** as follows:

[0017] FIG. 6 depicts a ~~cross-section~~ cross-section of a portion of the structure illustrated in FIG. 5, the ~~cross-section~~ cross-section being taken at line B-B of FIG. 5;

Please amend paragraph number **[0019]** as follows:

[0019] FIG. 8 depicts a ~~cross-section~~ cross-section of a portion of the structure illustrated in FIG. 7, the ~~cross-section~~ cross-section being taken at line C-C of FIG. 7;

Please amend paragraph number **[0021]** as follows:

[0021] FIG. 10 depicts a ~~cross-section~~ cross-section of a portion of the structure illustrated in FIG. 9, the ~~cross-section~~ cross-section being taken at line D-D of FIG. 9;

Please amend paragraph number **[0022]** as follows:

[0022] FIG. 11 depicts a ~~cross-section~~ cross-section of the same structure illustrated in FIG. 6 after an additional material layer has been deposited over the semiconductor wafer;

Please amend paragraph number **[0024]** as follows:

[0024] FIG. 13 is a micrograph taken at higher magnification showing the same top view of the prior art overlay target depicted in FIG. 12 after the semiconductor wafer has been subjected to a cleaning process;

Please amend paragraph number **[0026]** as follows:

[0026] ~~FIG. 15 - FIG.~~ FIGS. 15 through 18 illustrate various structures at different steps of a method according to the first embodiment of the method of the present invention; and

Please amend paragraph number **[0027]** as follows:

[0027] ~~FIG. 19 - FIG.~~ FIGS. 19 through 22 illustrate various structures at different steps of a method according to the second embodiment of the method of the present invention.

Please amend paragraph number **[0029]** as follows:

[0029] In a first embodiment, illustrated in drawing FIG. 5, the overlay target 30 of the present invention includes a continuous trench 32 having a plurality of raised lines or substantially vertically extending ribs or protrusions 34 disposed therein or from the bottom of the trench thereof. As can be seen in drawing FIG. 6, a ~~cross-section~~ cross-section of the overlay target 30 taken at line B-B of drawing FIG. 5, the raised lines 34 disposed within the continuous trench 32 originate at the bottom surface 36 of the continuous trench 32 and are defined by alternating spaces 38 etched into surface 39 of a first material layer 40 deposited over the semiconductor wafer 42. ~~Although, drawing~~ Although drawings FIG. 5 and ~~drawing~~ FIG. 6 illustrate an overlay target 30 including only a single continuous trench 32 forming a generally rectangular pattern, it should be understood that one or more continuous trenches may be used to

form an overlay target of the present invention and that such trenches may be configured in a variety of shapes or sizes to meet any particular processing need.

Please amend paragraph number **[0030]** as follows:

[0030] In another embodiment illustrated in drawing FIG. 7, the overlay target 30 includes a plurality of discontinuous trenches 44 creating a pattern that can be evaluated by a registration tool. The discontinuous trenches 44 of the second embodiment each include a series of raised lines 34, and as can be clearly seen in drawing FIG. 8, a ~~cross-section~~ cross-section taken at line C-C of drawing FIG. 7, the raised lines 34 originate from the bottom surfaces 46 of each discontinuous trench 44 and are defined by alternating spaces 38 etched into the surface 39 of a first material layer 40 deposited over the semiconductor wafer 42. Although the discontinuous trenches 44 of the overlay target 30 illustrated in drawing FIG. 7 form a generally rectangular outline, it should be understood that the overlay target of the present invention may also include a plurality of discontinuous trenches disposed in any other pattern suitable for a particular fabrication process or registration tool.

Please amend paragraph number **[0031]** as follows:

[0031] A third embodiment of the overlay target 30 of the present invention is illustrated in drawing FIG. 9. The third embodiment of the overlay target of the present invention is similar to the previous two embodiments except that instead of continuous or discontinuous trenches, the overlay target 30 of the third embodiment includes a pad area 48 including a plurality of raised lines 34 defined by a plurality of alternating spaces 38 etched into the surface 39 of a first material layer 40 deposited over a semiconductor wafer 42 (as shown in drawing FIG. 10, a ~~cross-section~~ cross-section taken at line D-D of drawing FIG. 9). As can be seen in drawing FIG. 10, the raised lines 34 within the pad area 48 originate at the bottom surface 50 of the pad area 48.

Please amend paragraph number **[0033]** as follows:

[0033] The spaced raised lines included in each of the trenches or pad areas of an overlay target of the present invention substantially prevent overlying material layers from conforming to the topography of the overlay target. Illustrated in drawing FIG. 11 is the same ~~cross-section~~ cross-section of material illustrated in drawing FIG. 6 after a second material layer 52 has been deposited over the surface 39 of the first material layer 40, which has been etched to include the overlay target 30. The spaces 38 defining the raised lines 34 of the overlay target of the present invention are sufficiently narrow so that the second material layer 52 does not substantially conform to the topography of the overlay target 30. As a result, the topography of the overlay target 30 is not transferred to the second material layer 52, and the top surface 54 of the second material layer 52 does not include depressions which collect process residue in sufficient quantities to interfere with the operation of a registration tool. Therefore, the raised lines of the overlay target of the present invention ~~eliminates~~ eliminate periodic cleaning steps which would otherwise be necessary to ensure the overlay targets ~~may be~~ are accurately evaluated by a registration tool.

Please amend paragraph number **[0035]** as follows:

[0035] Although ~~drawing~~ drawings FIG. 5 through ~~drawing~~ FIG. 11 depict overlay targets etched into the first material layer applied over a semiconductor wafer, it should be understood that the overlay target may also be etched directly into the surface of the semiconductor substrate. Alternatively, as two or more sets of overlay targets are generally used to complete fabrication of state of the art semiconductor devices, an overlay target according to the present invention may also be created in material layers deposited after a first material layer has been deposited and processed as needed.

Please amend paragraph number **[0036]** as follows:

[0036] A useful comparison is illustrated in ~~drawing~~ drawings FIG. 12, FIG. 13 and FIG. 14 showing the desirability of an overlay target according to the present invention.

Provided in drawing FIG. 12 is a micrograph of a top view of a trench-type overlay target as seen through a subsequently applied material layer. The continuous trench forming the overlay target of drawing FIG. 12 lacks the raised lines of the overlay target of the present invention and, therefore, the topography of the trench has transferred to the top surface of the subsequently applied material layer, resulting in a depression in the top surface of the subsequently applied material layer corresponding to the trench forming the overlay target. As can be seen in drawing FIG. 12, during a polishing step, process residue, HSG Poly in this case, has collected in the depression corresponding to the overlay target trench, and the outline of the overlay target appears ragged and inconsistent.

Please amend paragraph number **[0039]** as follows:

[0039] The present invention also includes a method for forming an overlay target, which will be described in relation to ~~drawing~~ drawings FIG. 15 through ~~drawing~~ FIG. 22. A first embodiment of the method of the present invention includes providing a semiconductor substrate 60 having top surface 62 and a bottom surface 64. The semiconductor substrate 60 may be made from any suitable material, such as silicon, gallium, or sapphire materials, and the semiconductor substrate 60 may include one or more doped regions. A material layer 66, such as a borophosphosilicate glass layer or other dielectric, is then deposited over the top surface 62, and a layer of resist 68 is deposited over the material layer 66. The layer of resist 68 may include any suitable resist known in the art, and the resist layer may be applied by any known means, such as known spin coating processes. As shown in drawing FIG. 16, the layer of resist 68 is then exposed and developed as is known in the art to provide a resist pattern 70 that will result in a desired overlay target. The material layer 66 deposited over the top surface 62 of the semiconductor substrate 60 is then etched, for example, by an NF_3 or a chlorine etch, providing an overlay target 72 of the present invention including a plurality of raised lines 74, as can be seen in ~~drawing~~ drawings FIG. 17 and ~~drawing~~ FIG. 18, a ~~cross-section~~ cross-section taken at line E-E of drawing FIG. 17.

Please amend paragraph number **[0041]** as follows:

[0041] In a second embodiment of the method of the present invention the overlay target is etched directly into the semiconductor substrate 60. Thus, as is shown in drawing FIG. 19, the method according to the second embodiment requires providing a semiconductor substrate 60 having a top surface 62 and a bottom surface 64 and depositing a ~~resist~~ layer of resist 68 over the top surface 62 of the semiconductor substrate 60. Again the semiconductor substrate 60 may constitute any suitable semiconductor material, such as those described in relation to the first embodiment. Further, any suitable resist, such as those already described, may be used, and the ~~resist~~ layer of resist 68 may be deposited by any appropriate method for the resist material used, such as spinning. After the ~~resist~~ layer of resist 68 is deposited, the ~~resist~~ layer of resist 68 is exposed and developed as is known in the art to form a resist pattern 70 (shown in drawing FIG. 20) that will result in a desired overlay target after etching. The semiconductor substrate 60 is then etched by any known process suitable for the material used to form the semiconductor substrate 60, for example, an NF_3 or a chlorine etch. As can be seen in ~~drawing~~ drawings FIG. 21 and ~~drawing~~ FIG. 22, a ~~cross-section~~ cross-section of drawing FIG. 21 taken at line F-F, etching the semiconductor substrate 60 provides an overlay target 72 according to the present invention including a plurality of raised lines 74.